AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1 - 20. (canceled)

21. (currently amended) A signal processing integrated circuit comprising at least one channel and each channel ~~a plurality of channels~~ comprising at least one input ~~a plurality of inputs~~ coupled to a plurality of amplifiers ~~plurality of amplifiers~~, wherein the amplifiers process ~~amplify~~ at least one input signal ~~any signals~~ coming to the ~~plurality of~~ inputs, each channel further ~~input amplifier is part of a channel of said plurality, said readout channels~~ comprising:

~~a means for receiving one or more input signals;~~

at least one amplifier selected from said plurality of amplifiers ~~an amplifier~~ coupled to at least one of the said inputs ~~input~~ for processing ~~integrating~~ said ~~one or more~~ input signals and outputting the ~~an~~ amplified signal;

a processing circuit for further processing the said amplified signal and outputting the processed signal ~~amplifier output~~, ~~and~~

a trigger circuit to produce at least one trigger signal using the said processed signal and output the said trigger signals, and

an output circuit system ~~a means~~ for outputting said processed signals responsive to said input signals.

22. (currently amended) The integrated circuit ~~channel~~ of claim 21, wherein a polarity switching circuit is connected to said amplifiers ~~included~~.

23. (currently amended) The integrated circuit ~~channel~~ of claim 22, wherein said polarity switching circuit is externally controlled.

24. (currently amended) The integrated circuit ~~channel~~ of claim 21, further comprising a gain stage coupled to said amplifiers ~~charge sensitive amplifier~~.

25. (currently amended) The integrated circuit ~~channel~~ of claim 21, wherein at least one of the said amplifiers is ~~further comprising~~ a shaper amplifier to shape the said amplified signal to output a shaped signal ~~for providing shaped, integrated detector signals responsive to said selected signal~~.

26. (currently amended) The integrated circuit ~~channel~~ of claim 25, wherein said shaped~~, integrated detector~~ signal is of an approximately inverted bell shaped form.

27. (currently amended) The integrated circuit ~~channel~~ of claim 25, wherein said shaped~~, integrated detector~~ signal is of an approximate uninverted bell shaped form.

28. (currently amended) The integrated circuit ~~channel~~ of claim 21, further comprising a peak hold or sample and hold circuit coupled to output of at least one of said amplifiers ~~amplifier~~.

29. (currently amended) The integrated circuit ~~channel~~ of claim 21, further comprising a plurality of comparators connected to said amplifiers.

30. (currently amended) The integrated circuit ~~channel~~ of claim 29, wherein the said comparators can be at least one of following types; ~~a~~ leading edge, ~~a~~ zero crossing, ~~or~~ ~~a~~ constant fraction ~~type or a mixture of such~~ comparators.

31. (currently amended) The integrated circuit ~~channel~~ of claim 29, wherein said plurality of comparators enclose at least one ~~predetermined~~ pulse height range of the said input signals ~~energy band~~.

32. (currently amended) The integrated circuit ~~channel~~ of claim 30, further comprising a ~~differentiator~~ circuit coupled to at least one of said ~~first~~ plurality of comparators, said

~~differentiator~~ circuit producing a fast trigger signal output ~~with low jitter~~.

33. (currently amended) The integrated circuit ~~channel~~ of claim 28, ~~wherein~~ further comprising a circuit to connect an output of said peak hold or sample and hold circuit ~~is~~ one at a time to an output ~~multiplexed to said means for outputting~~.

34. (currently amended) The integrated circuit ~~channel~~ of claim 29, wherein an output of at least one of said plurality of comparators initiates a readout cycle of said signal processing ~~data readout~~ integrated circuit.

35. (currently amended) The integrated circuit ~~channel~~ of claim 21, wherein said trigger circuit ~~data outputting means~~ outputs a trigger ~~readout~~ signal for at least one channel of said plurality of integrated circuit channels processing ~~containing~~ an input signal.

36. (currently amended) The integrated circuit ~~channel~~ of claim 35, wherein said output circuit system ~~data outputting means~~ only outputs said readout signal for said channel of said plurality of integrated circuit channels for which a said trigger signal has been received.

37. (currently amended) The integrated circuit ~~channel~~ of claim 35, wherein said output circuit system ~~data outputting means~~ outputs said processed ~~readout~~ signal ~~for~~ from at least one of the said channel of said plurality of integrated circuit channels after at least one the said trigger signal has been produced ~~received~~ for any one of said plurality of integrated circuit channels.

38. (currently amended) The integrated circuit ~~channel~~ of claim 37, wherein said trigger signal is an external trigger signal.

39. (currently amended) The integrated circuit ~~channel~~ of claim 21, wherein said output circuit system ~~data outputting means~~ outputs a readout signal for one triggered channel of said plurality of integrated circuit channels and disables all remaining channels of said plurality of integrated circuit channels, wherein a time delay between said readout signal and said disablement of said remaining channels is controlled by an externally supplied signal.

40. (currently amended) The integrated circuit ~~channel~~ of claim 21, wherein the said at least one amplifier coupled to the said input is a charge sensitive amplifier ~~type~~.

41. (currently amended) The integrated circuit ~~channel~~ of claim

21, wherein the said amplifier connected to the said inputs changes the signal into a voltage output ~~type~~.

42. (currently amended) The integrated circuit ~~channel~~ of claim 40, wherein said ~~input~~ charge sensitive amplifier has an active or passive resistive feedback circuit.

43. (currently amended) The integrated circuit ~~channel~~ of claim 21, wherein the said amplifier is a current integrating type.

44. (currently amended) The integrated circuit ~~channel~~ of claim 29, further comprising a first comparator of said plurality of comparators is a low level discriminator, and

wherein at least one of said first comparator produces ~~allows~~ an output trigger when pulse height of the said processed input signal ~~a peak hold circuit output~~ is larger than a first threshold voltage.

45. (currently amended) The integrated circuit ~~channel~~ of claim 29, further comprising a second comparator of said plurality of comparators wherein said second comparator is an upper level discriminator, and

wherein said second comparator only produces ~~issues~~ a signal when pulse height of the said processed input signal ~~said peak hold circuit output~~ is larger than a second threshold voltage.

46. (currently amended) The integrated circuit ~~channel~~ of claim 21, further comprising circuitry for measuring the arrival time difference of said input signals between different channels.

47. (currently amended) The integrated circuit of claim 21, further comprising ~~includes~~ a control ~~and setting~~ circuit to control all the channels and their components, sets the settings and outputs the information.

48. (currently amended) The integrated circuit ~~channel~~ of claim 29, wherein the plurality of comparators is ~~can be~~ a single comparator.

49. (currently amended) The integrated circuit ~~channel~~ of claim 29, wherein at least one of the plurality of comparators is a ~~can be of~~ discriminator ~~type~~.

50. (currently amended) The integrated circuit ~~channel~~ of claim 29, wherein at least one of the plurality of comparators is a ~~may have at least one~~ fast comparator.

51. (currently amended) The integrated circuit ~~channel~~ of claim 35, wherein said output circuit system ~~data outputting means uses~~ provides sparse readout capability.

52. (currently amended) The integrated circuit ~~channel~~ of claim 51, wherein said sparse readout capability ~~also includes means to readout~~ selectively reads out ~~other~~ channels ~~which may also have signal which has~~ which have not produced a said trigger in that channel.

53. (currently amended) The integrated circuit ~~channel~~ of claim 21, further comprising circuitry for pole zero cancellation connected to the said amplifiers.

54. (new) The integrated circuit of claim 40, wherein the said charge sensitive amplifier is a self resetting type.

55. (new) The integrated circuit of claim 21, further comprising digital circuits for setting and controlling the said signal processing integrated circuit.

56. (new) The integrated circuit of claim 21, wherein all the channels and circuits are built onto silicon using processes that include at least one of the following processes; CMOS and BiCMOS.

57. (new) The integrated circuit of claim 21, wherein the said input signals come from a detector that include at least one of the following detector types; CdZnTe, CdTe, Si, GaAs, Selenium, PbI_2, HgI_2 and $CdWO_4$.

58. (new) The integrated circuit of claim 46, further comprising circuitry for measuring time difference of said input signals between different channels by measuring the phase difference of a Sine and Cosine wave simultaneously sent to each channel at the time when the said channel produces a trigger.